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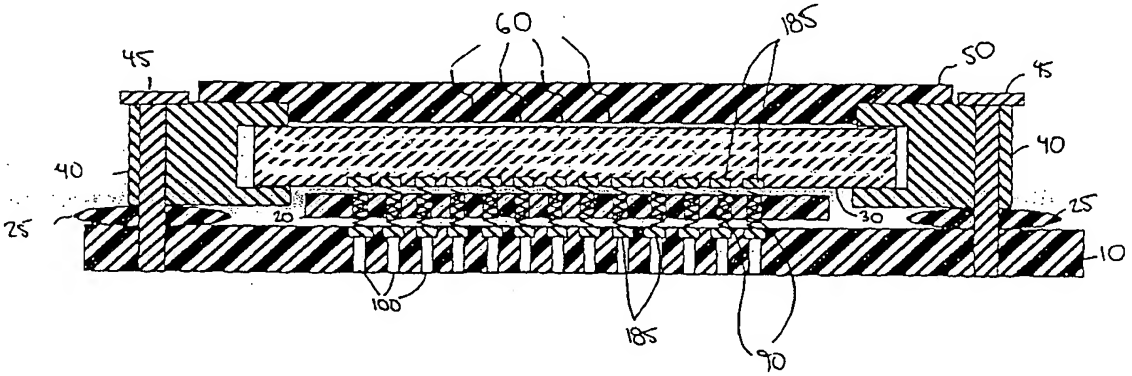
(54) Title: PLANARIZING INTERPOSER



(57) Abstract: A probe card assembly that compensates for differing rates of thermal expansion is comprised of a multi-layered dielectric plate (30) interposed between a probe head (50) and a printed circuit board (10). The printed circuit board (10) has upon its surface a first plurality of electrical contacts arranged in a pattern. The dielectric plate (30) has a second plurality of electrical contacts arranged in a pattern matching the first plurality of contacts. A planarizing interposer (20) is interposed between the plate (30) and the printed circuit board (10) and has a pattern of holes matching the pattern of electrical contacts on the printed circuit board and plate. The assembly further includes electrical connectors disposed within each of the holes arrayed in a pattern upon the planarizing interposer (20) conductive bumps (120) or fuzz buttons (90) making electrical contact with the first and second plurality of electrical contacts.

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PLANARIZING INTERPOSER

BACKGROUND OF THE INVENTION

This invention relates to the manufacture of probe card assemblies used to test the electrical continuity of integrated circuits formed on semiconductor wafers, such as silicon or gallium arsenide.

In the standard design of probe cards for performing such testing, a multi-layered ceramic (MLC) plate is inserted between a probe head that has a plurality of small diameter probes positioned to contact circuitry on an integrated circuit under test and a printed circuit board (PCB) that interfaces with an electric meter or other piece of test equipment. The plate is a space transformer having electrically conductive lines with conductive vias extending therethrough. The purpose of the MLC space transformer is to re-route electrical signals from the very finely pitched pattern of electrical contacts on the probe head to the more coarsely pitched pattern on the printed circuit board. By "pitched" it is meant that there exists spacing between adjacent lines or vias. In the process of testing an integrated circuit, electrical connection must be made between the MLC and the printed circuit board. Such a connection is typically achieved by soldering the MLC to the PCB using industry standard soldering techniques to form a rigid solder connection. When conducting such testing at elevated temperatures, for example between 75 degrees and 125 degrees Celsius, it is desirable to manufacture the probe head out of materials whose Coefficient of Thermal Expansion (CTE) closely matches that of silicon wafer being tested. The CTE of silicon is 3.2 ppm/degC. Accordingly, it is preferred that the CTE of the probe head be approximately 2 times that of silicon, such as less than 7 ppm/degC.

Because the MLC makes electrical contact with the finely pitched contacts on the probe head, it too must have a CTE closely matching that of silicon. Preferably, the CTE of the MLC is also within 2 times of the CTE of silicon. This requirement presents a problem when mating the MLC to the PCB, as the CTE of PCB is typically 17 ppm, much higher than that of silicon. Because of the differing rates of expansion between the MLC and the PCB, there is a potential for the rigid solder connections to crack under the mechanical stress that results from heating and/or cooling the structure.

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Typically, all probes of the probe head must be planar within a tolerance of a few thousandths of an inch. Careful control of manufacturing and assembly tolerances, as well as additional grinding and polishing processes, are required to maintain such a degree of planarity. Existing circuitry testing methods and apparatuses do not account for this difference of CTEs. For example US Patent No. 5,623,213 entitled "Membrane Probing of Circuits" and US Patent No. 5,841,291 entitled "Exchangeable Membrane Probe Testing of Circuits" are directed to the use of electrically conductive bumps on a flexible substrate or membrane to test electrical circuits. There is no suggestion or discussion that the system compensates for the differences of CTE inherent in the overall system.

Likewise, US Patent No. 5,973,504 entitled "Programmable High-Density Electronic Device Testing" is directed to a system for testing high-density electronic devices. More particularly, this patent discloses the use of a test system with a multi-chip module to route signals between pads of a device under test and a test circuit. This system employs a membrane probe card and conductive circuit connection bumps. The membrane probe card is screwed onto the housing using a frame ring and is positioned between a pressure mechanism and the device under test. The conductive bumps are grouped on the membrane to correspond with the connection pad arrays. In an alternative embodiment, electrical connection may be maintained using electrical button connectors. Again there is no suggestion that the system be designed to compensate for the differences of CTE inherent in the testing system.

Commonly owned US Patent Nos. 6,163,142 and 6,297,657, both entitled "Temperature Compensated Vertical Pin Probing Device," are directed to improved probing devices useful in testing integrated circuits over large temperature ranges. Both of these patents disclose methods and apparatuses complementary to the method and apparatus disclosed herein.

Accordingly, there is a need for a method and apparatus useful to adjust the planarity of the probe head after assembly in order to correct for misalignment. Ideally, such a method and apparatus should minimize the need for critical machining and assembly processes.

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BRIEF SUMMARY OF THE INVENTION

It is an object of the invention to find a method of electrically and mechanically connecting the MLC to the PCB in a way that will allow for the differing rates of expansion while maintaining electrical contact.

Additionally, it is an object of the invention to provide a process whereby one may adjust the planarization of the MLC relative to the PCB.

One novel aspect of the present invention involves the attachment of the MLC to the PCB in a manner that allows for differing rates of thermal expansion as well as allowing for probe head planarization, while maintaining electrical contact between the MLC and the PCB.

To compensate for the differing rates of thermal expansion, the present invention suitably employs a planarizing interposer that includes a plate positioned between the MLC and the PCB while maintaining a compliant electrical connection. For the purposes of this disclosure, "compliant electrical connection" shall refer to a connection that maintains electrical connection and the integrity of the components on either side of the interconnection regardless of differing rates of thermal expansion, and allows for planarization of the head assembly. Compliant electrical connection with the device under test (integrated circuit) may be maintained using fuzz buttons or conductive bumps. In embodiments where fuzz buttons are used, the plate has a plurality of holes (also called vias or via holes) drilled in a pattern that matches the pattern of electrical contacts on the PCB. Fuzz buttons are then positioned within the holes. In embodiments where conductive bumps are employed, the conductive bumps are screened or deposited onto land grid array pads of the MLC and/or the PCB.

In a first embodiment, there is disclosed a probe card assembly for testing integrated circuits comprising: a multi-layered dielectric plate interposed between a probe head and a printed circuit board, the printed circuit board having arrayed upon its surface a first plurality of electrical contacts arranged in a pattern, the dielectric plate having arrayed upon its surface a second plurality of electrical contacts arranged in a pattern substantially matching the first plurality of electrical contacts; a planarizing interposer interposed between the ceramic plate and the printed circuit board, the planarizing interposer having a pattern of holes matching the pattern of electrical contacts on the printed circuit board and the dielectric plate; a mounting ring clamped to the plate and the mounting ring attached to

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the printed circuit board; and a third plurality of compliant electrical connectors disposed within a multiplicity of the holes arrayed in a pattern upon the planarizing interposer, the electrical connectors making electrical contact with the first plurality of electrical contacts and the second plurality of electrical contacts.

In a second embodiment, there is disclosed a method of adjusting the planarization of a probe card assembly comprising the steps of: (a) screwing the adjustment screws sufficiently tightly so as render the mounting ring in close proximity with the printed circuit board; (b) determining the planarization of said probe head; and (c) adjusting the tightness of the screws to achieve a desired degree of planarization for the probe head.

In a third embodiment, there is disclosed a method of assembling a probe card assembly comprising the steps of: (a) inserting each of a plurality of fuzz buttons into via holes using an electrically conductive tool; and (b) confirming electrical connectivity between the multi-layered dielectric plate and the printed circuit board.

In a fourth embodiment, there is disclosed a method of assembling the probe card assembly of claim 1, comprising the steps of: (a) providing a temporary plate to verify electrical connection; and (b) replacing the temporary plate with a multi-layered dielectric prior to testing.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of the probe card assembly according to the present invention.

Fig. 2 is a cross-sectional representation of the probe card assembly.

Fig. 3 is a cross-sectional representation of the probe card assembly depicting the use of fuzz buttons.

Fig. 3a is a cross-sectional representation of the probe card assembly with through holes in the PCB for alignment purposes.

Fig. 4 is a cross-sectional representation of the probe card assembly depicting the use of fuzz buttons with filled via holes.

Fig. 5 is a cross-sectional representation of the probe card assembly depicting the use of conductive bumps between the PCB and the space transformer.

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Fig. 6 is a cross-sectional representation of the probe card assembly depicting the use of conductive bumps between the PCB and MLC.

DETAILED DESCRIPTION

The present invention includes a planarizing interposer located between a MLC or other multi-layered dielectric and a PCB. The interposer uses a compliant interconnect (generally shown in Figure 1), such as fuzz buttons (illustrated in Figures 2, 3, and 4), a Pin Grid Array (illustrated in Figure 5), or conductive bumps (illustrated in Figure 6), to maintain electrical connection between the PCB and the MLC. Throughout this specification reference to a MLC is intended to also include other suitable multi-layered dielectric plates.

Turning to Figure 1, an interposer 20 includes a plate with a plurality of through-holes formed in a pattern that matches the pattern of a first plurality of electrical contacts on the PCB 10. Preferably, the plate is formed of a dielectric, such as rigid plastic. Most preferably, the plate is formed of Techtron PPS manufactured by Quadrant Engineering Plastic Products. The first plurality of electrical contacts are typically arranged in an array with pitch of 1.27 mm (0.05 inches). While 0.05 inches is typical, one skilled in the art would recognize that other pitches may be suitably employed. Electrical connectors are deposited in the through-holes to provide an electrical pathway. A preferred electrical connector is that of a small cylindrically shaped element called a fuzz button. The fuzz button is a commercial product consisting of a thin electrically conductive metal wire, such as beryllium copper, that has been compressed into a die to form a cylindrical mass and having spring-like properties. Examples of preferred fuzz buttons include those manufactured by Tecknit of Cranford, New Jersey.

The MLC 30 may be clamped to a mounting ring 40, which is then attached to the PCB 10 in a manner, as described below, that allows the ring's planarization to be adjusted. The mounting ring 40 is mounted to the PCB 10 using a plurality of screws 45. A preferred configuration employs three screws. On each screw, between the ring 40 and the PCB 10, are placed stiff springs 25, as shown in Figure 2. Suitable stiff springs include spring washers, such as Belleville washers manufactured by HK Metalcraft Inc. of Lodi, New Jersey. Most preferably, the screws 45 pass through the mounting ring 40 and spring washer 25, such that turning the screws allows the planarity of the mounting ring to

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be adjusted.. The MLC 30 may optionally rest on a shelf 55 in the mounting ring 40. Preferably, the MLC 30 is clamped onto the shelf in the ring.

Preferably, the mounting ring 40 is attached so that the MLC 30 is in close proximity with the surface of the PCB 10. The resulting compression causes the MLC 30 to be held in the ring against the fuzz buttons 90 (as shown in Figure 2) in the interposer 20. As a result, the fuzz buttons make electrical connection between the MLC 30 and the PCB 10. Since the electrical connection is not rigid, the PCB 10 is free to expand at a different rate than the MLC 30 while continuing to make electrical contact. A probe head (also called a test head) 50 (shown in Figure 2) can now be placed in a tester that determines the degree of planarization of the probe head 50. If adjustment is necessary, the appropriate adjusting screw 45 may be unscrewed slightly so as to level the probe head 50. The Belleville washers 25 are selected to provide sufficient pre-load between the ring 40 and the PCB 10 so as to ensure that the ring does not move under the normal loads applied during the probe test process. As shown in Figure 2, optional pads 185 may be deposited or brazed onto the MLC 30 or PCB 10

In an alternative embodiment, as shown in Figure 3, the PCB 10 has hollow plated vias or via holes 100. Fuzz buttons 90 are inserted in the via holes 100. Preferably, the fuzz buttons 90 have diameters slightly larger than the vias 100 so that the fuzz buttons 90 are held in place by compression. For example, the via holes 100 may be approximately 0.76 mm (0.03 inches) in diameter and the fuzz buttons 90 slightly larger. In this embodiment, no interposer (shown in Figure 2 as numeral 20) is required, saving a significant portion of the cost of the interposer 20, and eliminating the need for alignment of the frame to the PCB 10. Accordingly, because alignment is inherently ensured, this embodiment has improved reliability.

Preferably, the fuzz buttons 90 are inserted from the non-test side 160 of the PCB 10 and are pushed through until an electrical contact is verified between the fuzz button 90 and the MLC 30. The non-test side refers to the side of the board opposite the test head 50. Such a configuration ensures that the final height of all the fuzz buttons 90 relative to the MLC 30 are nearly the same. To simplify the assembly process, it may be desirable to temporarily use an aluminum plate in place of the MLC. Use of such a plate simplifies the verification of an electrical connection. Preferably, a tool that is electrically conductive is used to push the fuzz buttons 90 through the vias 100, so that contact may be verified

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when there is a closed electrical path from the tool, through the fuzz button 90 to a temporary plate and back to the tool. This temporary plate (not shown) temporarily replaces the MLC 30 for purposes of loading the fuzz buttons 90 and is removed and replaced with the MLC 30. It may be desirable to make the temporary plate slightly thicker than the actual MLC 30, such that the fuzz buttons 90 are compressed against the temporary plate. Removing the plate and replacing it with the MLC 30 then allows the fuzz buttons 90 to relax slightly while maintaining electrical contact, thereby minimizing the compressive force exerted on the MLC 30.

This configuration ensures the alignment of the fuzz buttons 90 relative to the PCB 10. To further simplify the alignment of the MLC 30 to the fuzz buttons 90, additional pads 185 may be optionally employed to the MLC's contact array (not shown) on the side of the MLC opposite the test head 50. The pattern of the MLC contact array matches the LGA pattern on the PCB 10. Two corresponding holes in the PCB 10 may be used to sight through the PCB 10 to the pads. The MLC 30 may then be adjusted so as to center the pads in the hole. A preferred arrangement includes two alignment pins, such as those used in pin grid array MLC's, that are brazed to the pads. These pads pass through two corresponding additional via holes in the PCB 10, thereby aligning the MLC's LGA array to the PCB's via array.

In an alternative embodiment (not shown), the stiff Belleville washers 25 may be eliminated or replaced with lower-stiffness washers, and the planarizing screws 45 may be counter-sunk into the mounting ring. In this alternative embodiment, the ring may be free to float relative to the PCB 10 and self-planarize during testing, while the counter-sunk screws suitably re-center the ring when the test load is removed. The degree of float between the ring and the PCB is compensated by the compliant electrical contacts (fuzz buttons or conductive bumps).

Figure 3a depicts the use of site holes 200 to assist in the alignment of the assembly.

In another embodiment, as shown in Figure 4, longer and softer fuzz buttons may be used with a plurality of blind vias 110. In this embodiment, the non-test end 160 of the vias 110 are filled such that the depth of the vias allow a portion of the fuzz buttons to protrude beyond the PCB 10. In this embodiment, the diameter of the vias 110 may be

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larger than that of the fuzz buttons 90 as friction is no longer preferred to maintain the fuzz buttons 90 position.

In an alternate embodiment, as shown in Figure 5, an interposer 20 is constructed using a Pin Grid Array (PGA) 180 brazed to the contact pads of the MLC 30. The PGA mates with and is inserted into plated vias in the PCB. Spring washers 25 (such as Belleville washers) are placed under the mounting ring 40 at a plurality of locations, preferably three. Adjustment screws 45 (also shown in Figure 1) pass through the washers 25 to allow the planarity of the ring to be adjusted. Once properly planarized, the tips of the PGA, which protrude through the back side (non-test side) of the PCB, are soldered to the back side of the PCB vias 100. Optionally, to shorten the electrical path of the pins 180, a conductive paste, such as a conductive epoxy or solder, may be injected or screened into the vias on the test head side of the board. Preferably, the inside diameters of the vias are larger than the pins so that when the pins are inserted into the vias, the paste fills the space between the pins and the vias to create an electrical connection. Such a configuration shortens the electrical path so that shorter pins may be used. The MLC 30 may then be aligned using the method set forth above. Because an electrical connection has been created between the MLC 30 and the PCB 10, the test head may be mounted to the mounting ring and MLC 30, and a final planarity check may be done with the completed assembly. If necessary, the planarity may be adjusted. Once properly aligned, the assembly is cured, such as by a low temperature cure cycle, to set the conductive paste. Once planarity is verified, an epoxy filler may be injected under the MLC 30 to fill the gap between the MLC 30 and the PCB 10, increasing the bond strength between the MLC 30 and the PCB 10.

In an alternative embodiment as shown in Figure 6, fuzz buttons 90 may be replaced with compliant conductive bumps 120. These conductive bumps 120, preferably made of conductive epoxy, such as a metal or graphite polymer with an electrical resistivity less than 0.005 ohm-cm, are screened or deposited onto land grid array pads of the MLC 30 and/or the PCB 10. When the MLC 30 and PCB 10 are brought into contact, the bumps 120 form a compliant electrical path between the MLC 30 and the PCB 10. The test head (not shown) is then mounted to the mounting ring 40 and aligned with the MLC 30. The test head's planarity is then tested to ensure proper planarity and adjusted, if necessary, by turning the adjustment screw 45 (of Figure 1) to bring the high side of the

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head closer to the PCB 10. The PCB 10 and space transformer 130 are then heated until the epoxy is cured, so that the space transformer 130 is held to the PCB 10. An epoxy under-filler is then injected under the MLC 30.

Optionally, the conductive bumps may be made of a solder paste preferably using a low melting point solder, such as 100 degC. Preferably, the solder is solid at room temperature. As the temperature rises during testing, the solder softens and re-flows, eliminating mechanical stress while maintaining electrical contact. When cooled, the solder re-solidifies.

Thus, there has been shown and described an apparatus and method to planarize a probe card assembly prior to testing. One skilled in the art would recognize that other embodiments and modifications may be useful without detracting from the overall purpose of this invention. Any such modifications and applications recognized by one skilled in the art is intended to fall within the scope of this application.

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WHAT IS CLAIMED IS:

1. A probe card assembly for testing integrated circuits characterized by:

a multi-layered dielectric plate (30) interposed between a probe head (50) and a printed circuit board (10) said printed circuit board (10) having arrayed upon its surface a first plurality of electrical contacts arranged in a pattern, said dielectric plate (30) having arrayed upon its surface a second plurality of electrical contacts arranged in a pattern substantially matching said first plurality of electrical contacts;

a planarizing interposer (20) interposed between said dielectric plate and said printed circuit board (10) said planarizing interposer (20) having a pattern of holes matching the pattern of electrical contacts on said printed circuit board (10) and said dielectric plate (30);

a mounting ring (40) clamped to said plate (30) and said mounting ring (40) attached to said printed circuit board (10); and

a third plurality of compliant electrical connectors disposed within a multiplicity of said holes arrayed in a pattern upon said planarizing interposer (20) said electrical connectors making electrical contact with said first plurality of electrical contacts and said second plurality of electrical contacts.

2. The probe card assembly of claim 1, characterized in that said mounting ring (40) is attached to said printed circuit board (10) with a plurality of screws (45).

3. The probe card assembly of claim 2, characterized in that a washer (25) is interposed between each of said plurality of screws (45) and said printed circuit board (10).

4. The probe card assembly of claim 3, characterized in that each of said washer (25) is a spring washer.

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5. The probe card assembly of claim 4, characterized in that said electrical contacts are arranged in array having a pitch of approximately 1.27.

6. The probe card assembly of claim 4, characterized in that said second plurality of compliant electrical connectors is comprised of a plurality of fuzz buttons (90).

7. The probe card assembly of claim 1, characterized in that said plurality of screws (45) are counter-sunk into said mounting ring (40).

8. The probe card assembly of claim 1, characterized in that said printed circuit board (10) includes one or more via holes (100, 110).

9. The probe card assembly of claim 8, characterized in that said fuzz buttons (90) are inserted into said via holes (100, 110).

10. The probe card assembly of claim 9, characterized in that said fuzz buttons (90) have diameters larger than the diameter of said via holes (100, 110).

11. The probe card assembly of claim 8, characterized in that said one or more via holes are blind vias (110).

12. The probe card assembly of claim 11, characterized in that said fuzz buttons (90) are inserted into said blind vias (110).

13. The probe card assembly of claim 12, characterized in that said fuzz buttons (90) inserted so as to protrude above the printed circuit board (10) toward said multi-layered dielectric plate (30).

14. The probe card assembly of claim 1, characterized in that said third plurality of compliant electrical connectors is comprised of a plurality of conductive bumps (120) that are screened onto said first plurality of electrical contacts.

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15. The probe card assembly of claim 1, characterized in that said third plurality of compliant electrical connectors is characterized by a plurality of conductive bumps (120) that are deposited onto said first plurality of electrical contacts.

16. The probe card assembly of claim 15, characterized in that said planarizing interposer (20) wherein said first plurality of electrical contacts is characterized by one or more land grid array pads (180) and wherein said conductive bumps (120) are applied to said pads.

17. The probe card assembly of claim 16, characterized in that said conductive bumps (120) consist of solder paste.

18. The probe card assembly of claim 17, characterized in that said solder paste has a low melting point.

19. The probe card assembly of claim 18, characterized in that said solder paste has a melting point less than or equal to 100 degC.

20. The probe card assembly of claim 1, characterized in that said multi-layered dielectric plate (30) further includes a pin grid array brazed (180) to said plurality of contact pads.

21. A method of adjusting the planarization of a probe card assembly of claim 5 characterized by the steps of:

(a) screwing said screws (45) sufficiently tightly so as render said mounting ring (40) in close proximity with said printed circuit board (10);

(b) determining the planarization of said probe head (50); and

(c) adjusting the tightness of said screws (45) to achieve a desired degree of planarization for said probe head (50).

22. The method of claim 21, characterized in that said mounting ring (40) floats relative to the printed circuit board (10).

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23. The method of claim 22, characterized in that said screws (45) are counter-sunk and further comprising the step of re-centering the mounting ring (40) during testing using said counter-sunk screws (45).

24. A method of assembling the probe card assembly of claim 6, characterized by the steps of:

(a) inserting each of said plurality of fuzz buttons (90) into said via holes (100, 110) using an electrically conductive tool; and

(b) confirming electrical connectivity between said multi-layered dielectric plate (30) and said printed circuit board (10).

25. The method of claim 24, characterized in that said fuzz buttons (90) are inserted from the non-test side (190) of the printed circuit board (10).

26. A method of assembling the probe card assembly of claim 1, characterized by the steps of:

(a) providing a temporary plate to verify electrical connection; and

(b) replacing said temporary plate with said multi-layered dielectric (30) prior to testing.

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27. A probe card assembly for testing integrated circuits characterized by:

a multi-layered dielectric plate (30) interposed between a probe head (50) and a printed circuit board (10) said printed circuit board (10) having arrayed upon its surface a first plurality of electrical contacts arranged in a pattern, said dielectric plate (30) having arrayed upon its surface a second plurality of electrical contacts arranged in a pattern substantially matching said first plurality of electrical contacts;

a mounting ring (40) clamped to said plate (30) and said mounting ring attached to said printed circuit board (10); and

a plurality of fuzz buttons (90) arranged in a pattern corresponding to said first plurality of electrical contacts and said second plurality of electrical contacts making electrical contact with said first plurality of electrical contacts and said second plurality of electrical contacts.

28. A probe card assembly for testing integrated circuits characterized by:

a multi-layered dielectric (30) plate interposed between a probe head (50) and a printed circuit board (10) said printed circuit board (10) having arrayed upon its surface a first plurality of electrical contacts arranged in a pattern, said dielectric plate (30) having arrayed upon its surface a second plurality of electrical contacts arranged in a pattern substantially matching said first plurality of electrical contacts;

a mounting ring (40) clamped to said plate (30) and said mounting ring (40) attached to said printed circuit board; and

a plurality of conductive bumps (120) arranged in a pattern corresponding to said first plurality of electrical contacts and said second plurality of electrical contacts making electrical contact with said first plurality of electrical contacts and said second plurality of electrical contacts.

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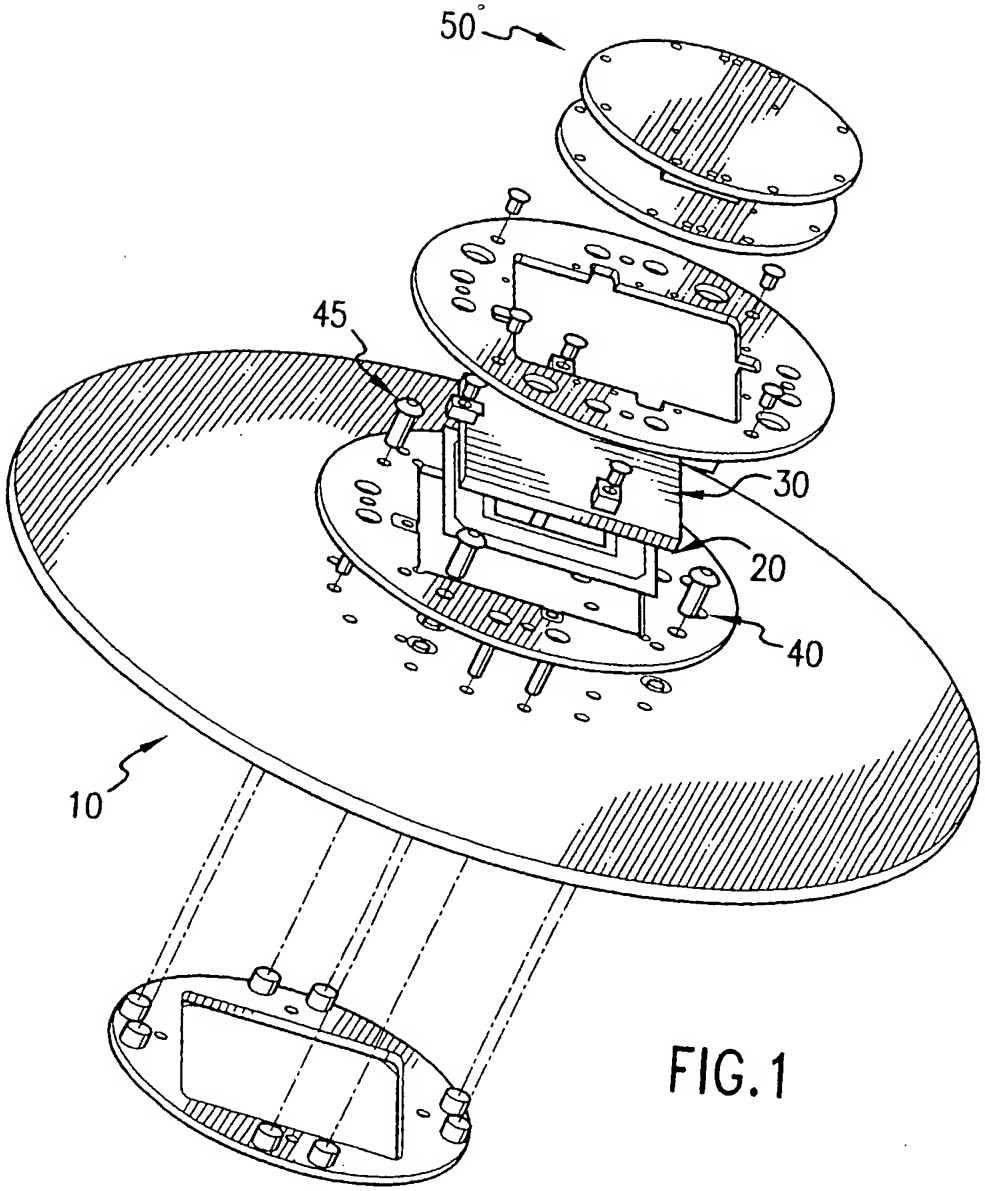

FIG.1

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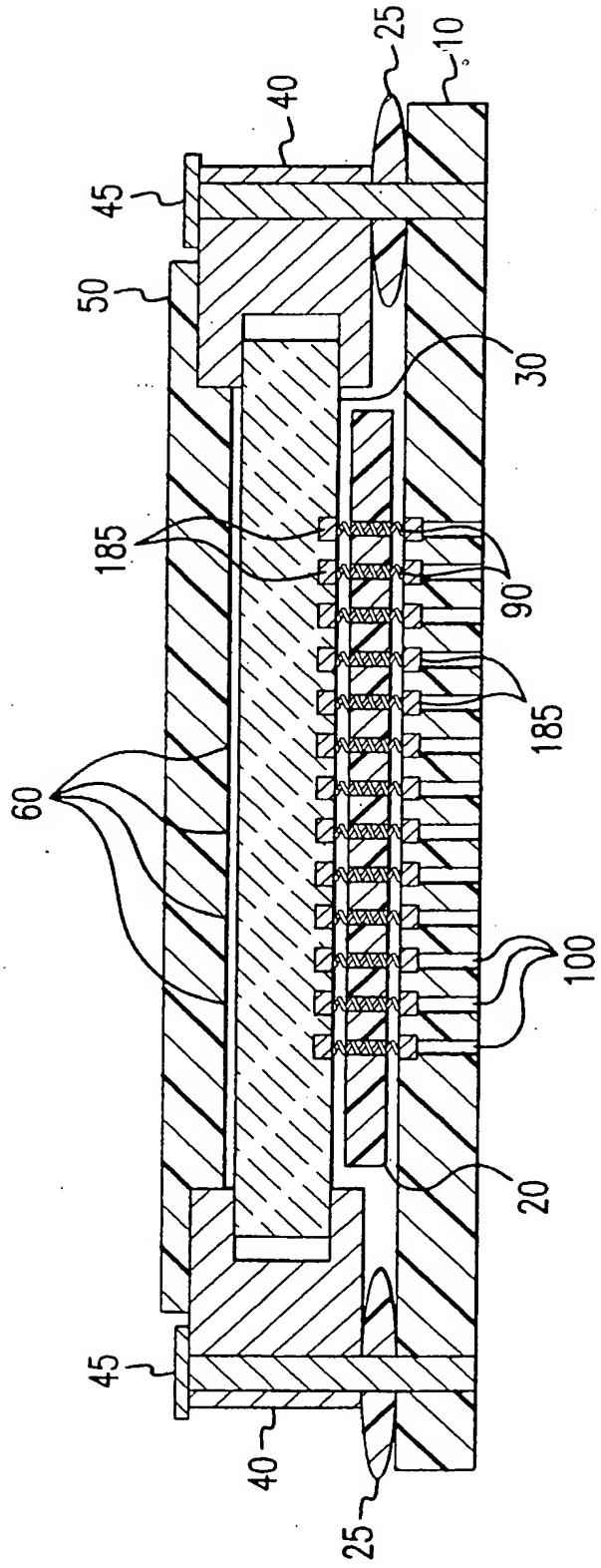

FIG.2

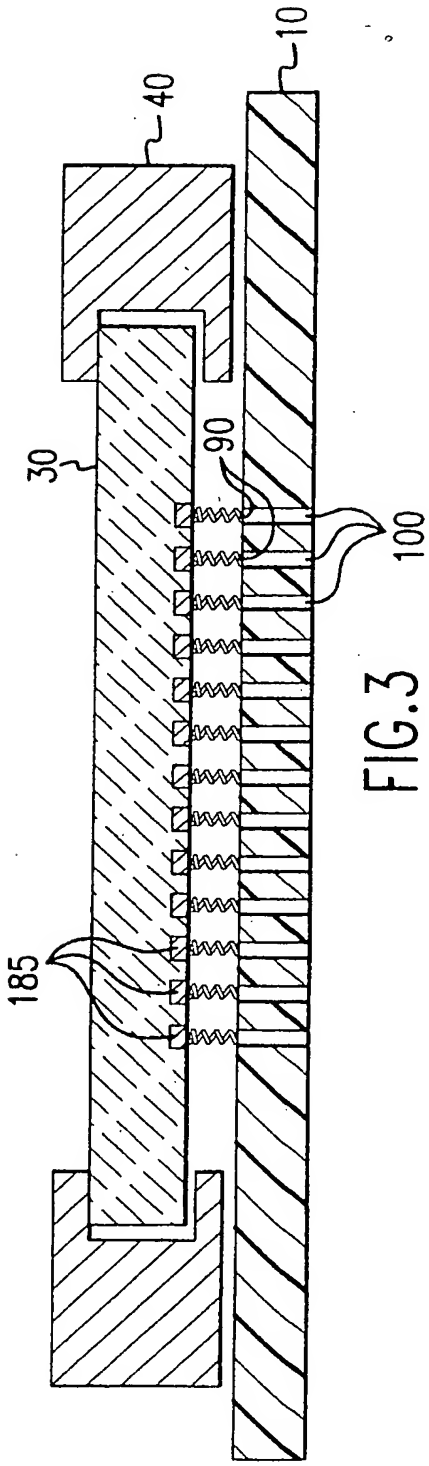

FIG.3

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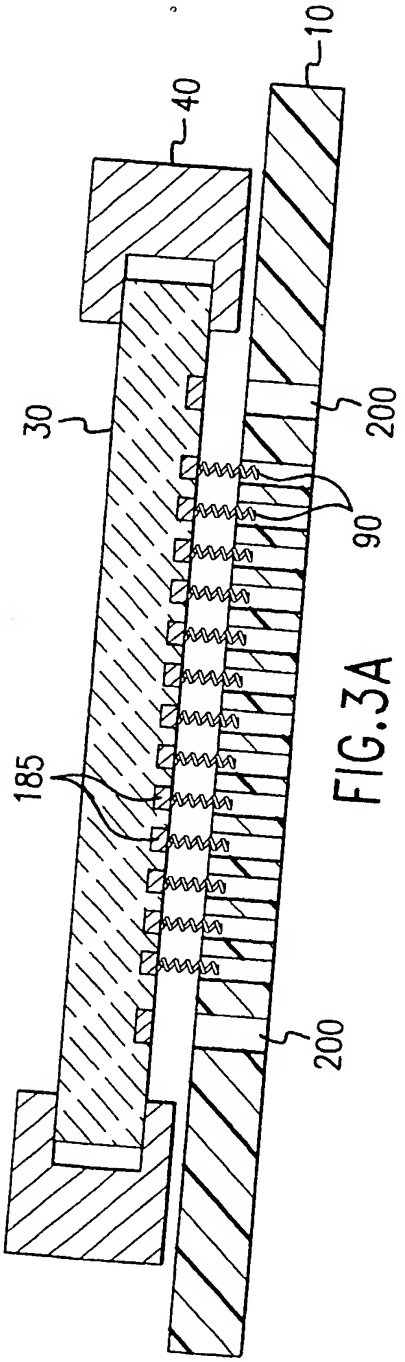

FIG.3A

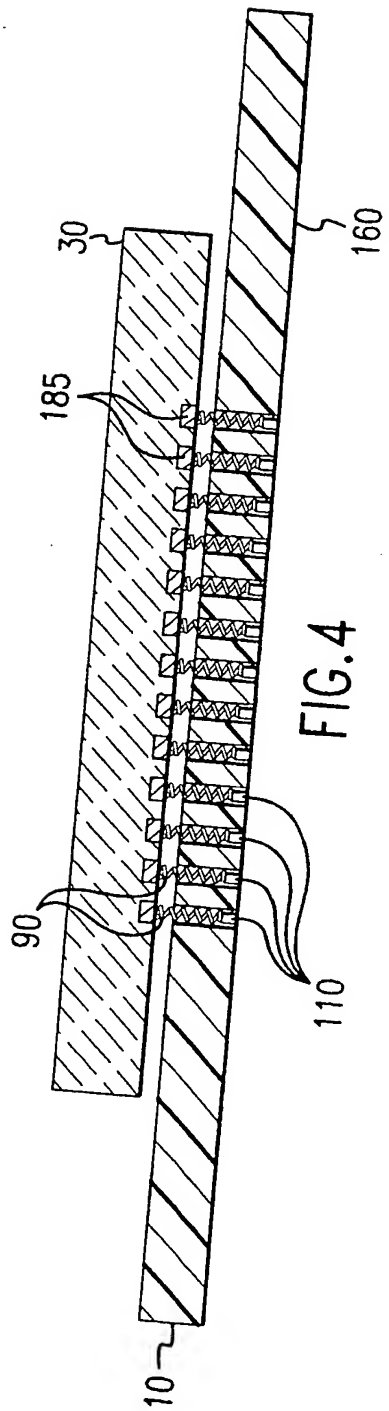

FIG.4

BNSDOCID: <WO_____02061442A1_I_>

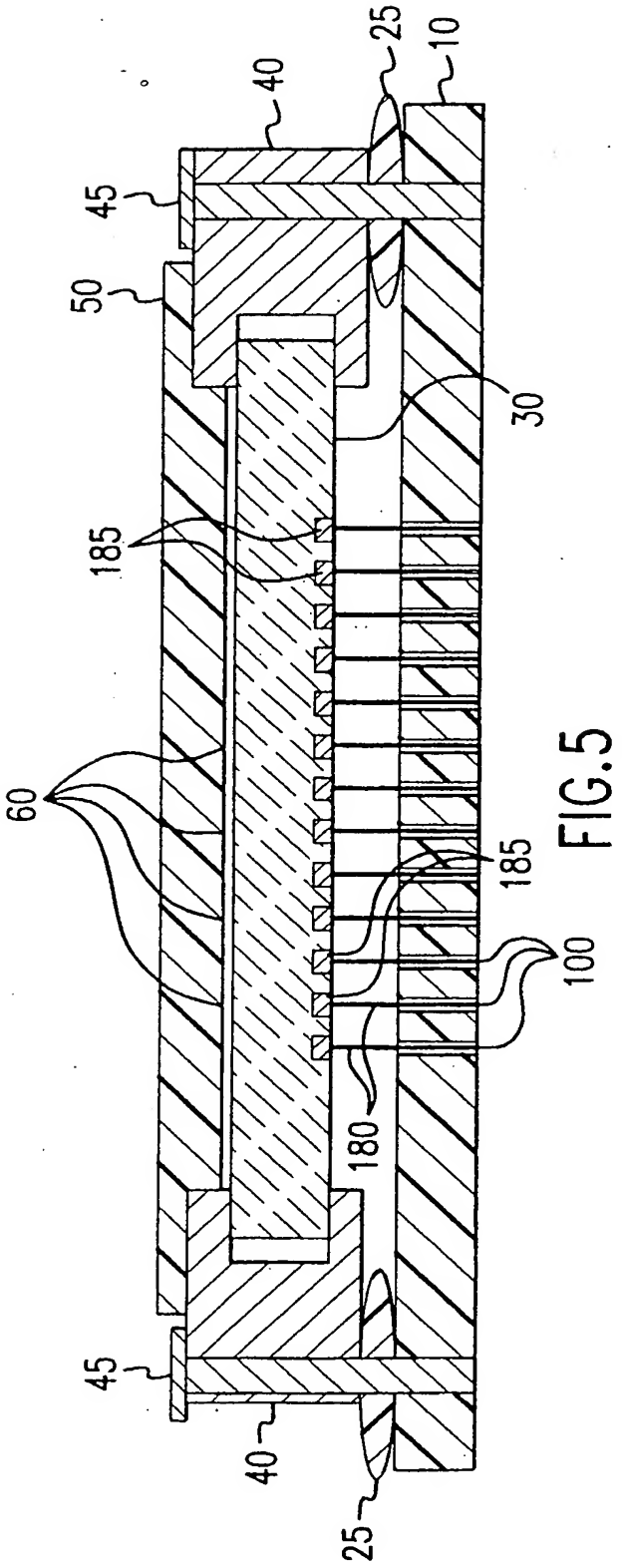

FIG.5

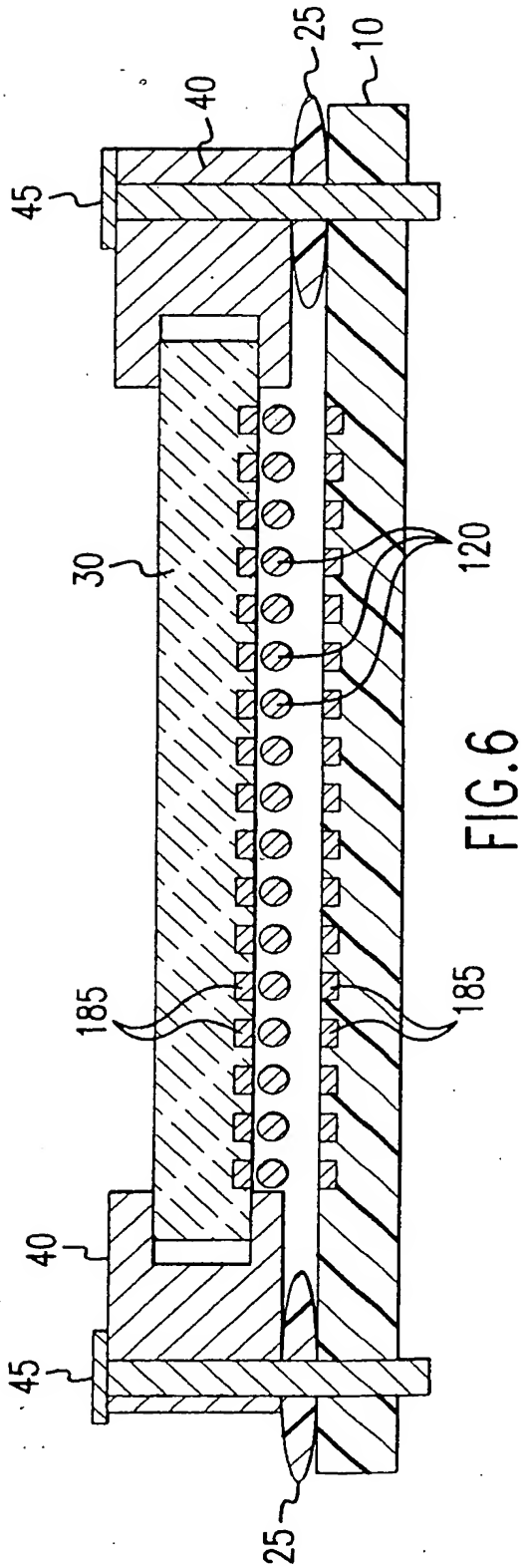

FIG.6

3NSDOCID: <WO 02061442A1 I >

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/02714

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) :G01R 31/02
US CL :324/758
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 324/754, 755, 757, 758, 765

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,440,240 A (WOOD ET AL) 08 AUGUST 1995 (08.08.1995), SEE ABSTRACT.	1-28
A	US 5,974,662 A (ELDRIDGE ET AL) 02 NOVEMBER 1999 (02.11.1999), SEE FIGURE 7.	1-28
A	US 6,133,744 A (YOJIMA ET AL) 17 OCTOBER 2000 (17.10.2000), SEE ABSTRACT.	1-28

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search
20 MAY 2002

Date of mailing of the international search report
21 JUN 2002

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